IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 20. (Cancelled)

21. (Original) A semiconductor device having a nonvolatile memory cell including first and second field effect transistors which are adjacent to each other, comprising:

(a) a first gate electrode as a gate electrode of said first field effect transistor, which is formed over a semiconductor substrate;

(b) a first semiconductor region of a first conduction type formed in said semiconductor substrate below said first gate electrode;

(c) a second gate electrode as a gate electrode of said second field effect transistor, which is formed over said semiconductor substrate; and

(d) a second semiconductor region of a second conduction type opposite to the first conduction type formed in said semiconductor substrate below said second gate electrode,

wherein a main surface of the semiconductor substrate in which said second semiconductor region is formed is formed so as to be lower than a main surface of the semiconductor substrate in which said first semiconductor region is formed.

22. (Original) A semiconductor device having a nonvolatile memory cell including first and second field effect transistors which are adjacent to each other, comprising:

(a) a first gate electrode as a gate electrode of said first field effect transistor, which is formed over a semiconductor substrate;

(b) a first semiconductor region of a first conduction type formed in said semiconductor substrate below said first gate electrode;

(c) a second gate electrode as a gate electrode of said second field effect transistor, which is formed over said semiconductor substrate via a gate insulating film; and

(d) a second semiconductor region of a second conduction type opposite to the first conduction type formed in said semiconductor substrate below said second gate electrode,

wherein an end portion of said second semiconductor region at the side of said second field effect transistor coincides with a position of an end portion of said second gate electrode at said first field effect transistor side and said gate insulating film or extends so as to be partly below a region of said second gate electrode and said gate insulating film.

23. (Original) The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming a channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing

to data storage is formed between a first gate electrode of said field effect transistor for a memory and a semiconductor substrate, and

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell.

24. (Original) The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said first semiconductor region has functions of a region for forming the channel of said field effect transistor for a memory and semiconductor regions for a source and a drain of said field effect transistor for selecting a memory cell, and

wherein said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell.

25. (Original) The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing

to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein said charge storage layer includes discrete trap levels.

26. (Original) The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and a semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein said charge storage layer is made of silicon nitride.

27. (Original) The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein a second gate electrode of said field effect transistor for selecting a memory cell is provided over said first gate electrode of said field effect transistor for a memory.

28. (Original) The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein the first gate electrode of said field effect transistor for a memory is provided over said second gate electrode of said field effect transistor for selecting a memory cell.

29. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between a gate electrode and a semiconductor substrate,

wherein a position of a side surface at an end in a width direction of said charge storage layer coincides with a position of a side surface at an end in a width direction of said gate electrode or is apart from the side surface at an end in the width direction of said gate electrode toward a center of said gate electrode.

30. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between a gate electrode and a semiconductor substrate,

wherein said charge storage layer is formed so that its whole region in plan view is included in a whole region of said gate electrode in plan view.

31. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein said n-type gate electrode has a first region near said charge storage layer and a second region as another region, and concentration of n-type impurity in said first region is lower than that of the n-type impurity in said second region.

32. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein concentration of n-type impurity in said n-type gate electrode is lower than that of the n-type impurity in a gate electrode of an n type in another field effect transistor provided over said semiconductor substrate.

33. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein concentration of n-type impurity in said n-type gate electrode is $1\times10^{18}/cm^3$ to $2\times10^{20}/cm^3$.

34. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein concentration of n-type impurity in said n-type gate electrode is $8\times10^{19}/cm^3$ to $1.5\times10^{20}/cm^3$.

35. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, or 34,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and charges in said charge storage layer are extracted to said memory gate electrode side, thereby erasing data.

36. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein electrons in said charge storage layer are extracted to said gate electrode side and positive holes in said gate electrode are injected to the charge

storage layer side and promoted to recombine with said electrons, thereby erasing data.

37. (Original) A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between a gate electrode and a semiconductor substrate,

wherein electrons in said charge storage layer are extracted to said gate electrode side, thereby erasing data, and said gate electrode is of a p type.

38. (Original) A semiconductor device having a nonvolatile memory cell in which data is erased by extracting charges stored in a charge storage layer to a gate electrode side,

wherein the lowest write level is higher than an initial threshold voltage of said nonvolatile memory cell.

39. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38, wherein said charge storage layer includes discrete trap levels.

40. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38, wherein said charge storage layer is made of silicon nitride.

41. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38, wherein said gate electrode is a memory gate electrode, and a

field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode.

42. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and

wherein a control gate electrode of said field effect transistor for selecting a memory cell is provided over said memory gate electrode.

43. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and

wherein said memory gate electrode is provided over a control electrode of said field effect transistor for selecting a memory cell.

44. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and

wherein a first semiconductor region of a first conduction type provided in a semiconductor substrate below said memory gate electrode has a function of a region for forming a channel of a first field effect transistor for a memory having said memory gate electrode and a function of semiconductor regions for a source and a drain of said field effect transistor for selecting a memory cell.

45. (Original) The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein a width of said gate electrode in a width direction of said gate electrode is larger than or equal to a width of said charge storage layer in the width direction of said gate electrode.